

IN THE SPECIFICATION

Please rewrite the title of the invention, at the top of page 1, so that it reads as follows:

SEMICONDUCTOR CIRCUIT WITH FLASH ROM AND IMPROVED SECURITY
FOR THE CONTENTS THEREOF

Please rewrite the paragraph at page 1, lines 5-9, so that it reads as follows:

Prior Art

Recently, a micro controller having a the function ~~for~~ of debugging programs by using JTAG (Joint Test Action Group) and the like has become ~~the~~ mainstream. Software developers debug application software by using this function to develop new programs easily.

Please rewrite the paragraph at page 1, lines 10-17, so that it reads as follows:

Also, a micro controller with flash ROM built-in has recently ~~increasing in number~~ become popular and can execute rewriting the flash ROM by using the JTAG. And a security bit is set in this flash ROM so that the contents of the flash ROM may not be read out by a third party. It is to be noted that the data written in the flash ROM is an application program created by the user of micro controller and that the writer in flash ROM cannot read out and rewrite partially the data by setting the security bit.

Please rewrite the paragraph at page 1, lines 18-25, so that it reads as follows:

AMENDMENT

(09/905,195)

However, although the contents of the flash ROM cannot be read out by the flash ROM writer in which the JTAG port is used after setting "1" ~~on~~ the security bit to "1", the contents of the flash ROM can be downloaded easily by the debugging function in which the JTAG port is used since a command can be inserted directly into a central processing unit (CPU). Therefore, the security bit of the conventional semiconductor circuit does not ~~function the security bit~~ enough to adequately protect the security of flash ROM.

Please rewrite the paragraph at page 1, line 26 through page 2, line 4, so that it reads as follows:

Summary of the Invention

The present invention has been achieved in ~~views~~ view of the aforementioned problem possessed by the conventional semiconductor circuit. A first object of the present invention is to provide a novel and improved semiconductor circuit capable of preventing the contents of flash ROM from being read out by the third party.

Please rewrite the paragraph at page 2, lines 10-13, so that it reads as follows:

To achieve the above object, according to a first aspect of the present invention, there is provided a semiconductor circuit wherein a JTAG control circuit controlled by the security bit of a flash ROM is equipped between the JTAG port and a TAP (Test Access Port).

Please rewrite the paragraph at page 2, lines 14-21, so that it reads as follows:

AMENDMENT

(09/905,195)

According to a second aspect of the present invention, there is provided a semiconductor circuit comprising: an inhibit (INHIBIT) NAND gate; a Pin scramble-circuit decoding a micro controller general-purpose port, which are set between the security bit of a flash ROM and the JTAG control circuit; and a circuit wherein the inverted level of the one of the Pin scramble-circuit output is input the one side of the inhibit NAND gate and the output of the security bit of a flash ROM is input the other side of the inhibit NAND gate.

Please rewrite the paragraph at page 2, lines 22-29, so that it reads as follows:

According to a third aspect of the present invention, there is provided a semiconductor circuit comprising: an inhibit NAND gate; a debug enable (DBG_EN) register as an internal register of the micro controller, which are set between the security bit of a flash ROM and the JTAG control circuit; and a circuit wherein the inverted level of the one of the debug enable register output is input the one side of the inhibit NAND gate and the output of the security bit of a flash ROM is input the other side of the inhibit NAND gate.

Please rewrite the paragraph at page 2, line 30 through page 3, line 9, so that it reads as follows:

According to a fourth aspect of the present invention, there is provided a semiconductor circuit having a security releasing means comparing the data which is input a test port with the data stored in a memory device and turning on a switch when the two data agree, and the semiconductor circuit comprising: a memory device to store control program and data; a central

AMENDMENT

(09/905,195)

processing unit to execute a specific process according to the program; a test port to input and output test signals; and a switch to control on/off between the test port and the memory device and/or the central processing unit according to the security bit set in a nonvolatile register.

Please rewrite the paragraph at page 3, lines 10-17, so that it reads as follows:

According to a fifth aspect of the present invention, there is provided a semiconductor circuit comprising: a memory device to store control program and data; a central processing unit to execute a specific process according to the program; a test port to input and output test signals; a switch to control on/off between the test port and the central processing unit; and a security releasing means comparing data which is input a test port with data stored in a memory device and turning on a switch when the two data agree.

Please rewrite the paragraph at page 4, lines 6-11, so that it reads as follows:

Detailed Description of the Preferred Embodiments

Hereinafter, the preferred embodiments of the semiconductor circuit of the present invention will be described in detail with reference to the accompanying drawings. The same reference numerals are attached to components having the same functions in following description and the accompanying drawings and a description thereof is omitted.

Please rewrite the paragraph at page 4, lines 12-15, so that it reads as follows:

(First Embodiment)

Fig. 1 illustrates a the general configuration of a JTAG (Joint Test Action Group) circuit wherein ~~following numerals correspond:~~ reference number 11 corresponds to a JTAG port; 13

AMENDMENT

(09/905,195)

and 14 correspond to TAP (Test Access Port); 16 corresponds to CPU; and 18 corresponds to a flash ROM.

Please rewrite the paragraph at page 4, lines 16-19, so that it reads as follows:

In this embodiment, as shown in Fig. 2, a JTAG control circuit 12 capable of prohibiting or allowing communication of signals is installed between the JTAG port 11 and the ~~TAP~~ TAPs 13 and 14, and is controlled by the security bit of the flash ROM 18.

Please rewrite the paragraph at page 4, line 22 through page 5, line 1, so that it reads as follows:

A programmer debugs and develops a program by using the JTAG port 11. When the development ends, he writes "1" in the security bit of the flash ROM 18 to input the JTAG control circuit 12 as a prohibit signal and the communication of signals is to be prohibited. As a result, the debugging function in which the JTAG port 11 is used cannot be used. In other words, the circuit is configured so that the security bit written "1" by inserting an OR gate for which an AND gate can be substituted in changing logic makes the ~~TAP~~ TAPs 13 and 14 inputted only "1".

Please rewrite the paragraph at page 5, lines 2-6, so that it reads as follows:

In this embodiment, since the JTAG port 11 is used not only for reading out by ~~the~~ a flash ROM writer ~~in which the JTAG port 11 is used~~ but also for the debugging function ~~in which~~ and

since the JTAG port 11 is ~~used~~ ~~are not become available~~ made unavailable by writing "1" in the security bit of the flash ROM 18, the contents of the flash ROM 18 cannot be read out by ~~the a~~ third party at all.

Please rewrite the Abstract, on page 22, as shown on a separate page that is attached to this Amendment. (A clean copy of the Abstract, without markings to show the changes, is also attached).